Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **N/C**
2. **AD**
3. **J1**
4. **J2**
5. **J3**
6. **Q**
7. **GND**
8. **Q**
9. **K1**
10. **K2**
11. **K3**
12. **CP**
13. **SD**
14. **VCC**

**.055”**

**.055”**

**12 11 10 9 8**

**3 4 5 6**

**7**

**13**

**14**

**2**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .055” X .055” DATE: 11/30/16**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: 54H72**

**DG 10.1.2**

#### Rev B, 7/1